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Digital Logic Design Midterm #1 Problems Points 1 . 3 2 . 4 3 . 6 4 . 2 Total 15 yes no Was the exam fair ? The University of Toledo s17m1s_dild7.fm - 2 EECS:1100 Digital Logic Design Dr. Anthony D. Johnson Student Name_____ 2/16/17 ...

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Digital Logic Design Midterm #1
Digital Logic Design (CS123) Midterm Assignment 1 Name: Shereen Faruqi Roll Number: 19B-094-SE Section: B Implementing XOR Gate using NAND Gates AX1 (A.

Digital Logic Design (CS123) Midterm Assignment 1 ...
View Test Prep - Fall 2016 Midterm 1 Practice - JaJa from ENEE 244 at University of Maryland, College Park. ENEE244: Digital Logic Design Spring 2016 Midterm I 1. (a) [16pt] Show how to convert

Fall 2016 Midterm 1 Practice - JaJa - ENEE244 Digital Logic...
Tuesday, Friday: 3 (12:00 – 1:20 p.m.) in SEC-111. Course Description: Overall Educational Objective: The student will develop the ability to design both combinational and sequential digital logic circuits. He will learn to design with common library hardware components.

Course: Digital Logic Design - course home page (Rutgers ...
Intro, Boolean Algebra, Comb Logic Design : Vahid 1.1-1.3, 2.1-2.5, Apendix A and B: 4/2 Wed : Combinational Logic Design : Vahid, 2.5-2.13, 3.1-3.2 **4/3 Th: Discussion meeting : Sequential Logic Design : 4/7 Mon : Quiz 1 (Covers Chapters 1 and 2.1-2.7) Solution **4/8 Tu : Flip Flops and FSMs : Vahid 3.3-3.4 **4/10 : Controllers and Sequential ...

CS 151 SQ08 Digital Logic Design
EECS:1100 Digital Logic Design Dr. Anthony D. Johnson Student Name _____ Problem 1 5 points Given is the logic circuit model of a state machine shown in Figure 1.1. Figure 1.1 A state machine with two flip-flops in its internal state memory block. (a)Logical model of the circuit.

Digital Logic Design Midterm #2
UNC- Charlotte ECGR 2181 - Fall 2009 - Logic Systems Design I Recitation - All Sections: 8:00 - 10:45 F, Woodward 125 Lecture: Section 001: 9:30 - 10:45, M/W, Woodward 140

ECGR2181 - Logic Systems Design I - Exams
Reconfigurable Logic, VHDL, IP cores, Embedded Systems. LABORATORY. Hardware: . Nexys TM-4 DDR Artix-7 FPGA Board (which houses the XC7A100T-1CSG324 Artix-7 FPGA): webpage; Nexys-4 DDR Schematics; Nexys-4 DDR Reference Manual

Fall 2016 - ECE278: Digital Logic Design
Digital Logic I EE 2720-2 Midterm Examination 102 9 November 2011, 14:40–15:30 CST Exam Rules Use only a pencil or pen. No calculators of any kind are allowed. Texting is out of the question. Alias Saila Problem 1 (22 pts) Problem 2 (22 pts) Problem 3 (22 pts) Problem 4 (12 pts) Problem 5 (12 pts)

Digital Logic I EE 2720-2 Midterm Examination
ICS 151 Digital Logic Design, Spring Quarter 2006, Midterm Page 3 Q2: FSM Design [20 points] Design a state diagram for a recognizer that recognizes an input sequence 11101. It has an input X and output Y. The recognizer sets the output to 1 (Y = 1) for exactly one clock cycle if the last five values on the input X were 11101

Spring 2006
Midterm 1 25 % (Wednesday, Mar 2, 4.00 p.m.) ... CpE 100: Digital Logic Design I Course Description CATALOG DATA Digital design concepts and fundamentals. Combinational circuits. MSI and LSI circuits. Sequential

machine fundamentals sequential circuit analysis and design. Modern developments.

CpE 100: Computer and Logic Design I
f16m2s_dild7.fm the university of toledo eecs:1100 digital logic design dr. anthony johnson student name digital logic design midterm problems points total 15

Midterm 2 sol - EECS 1100 Digital Logic Design - StuDocu
computer-aided design (CAD) logic simulation digital data transmission analog and digital converters digital displays The EE 121 lab has seven stations, each with a Pentium III PC, a C.A.D.E.T. board from E&L Instruments, an HP 54601 digital oscilliscope, an HP 3312 function generator, a FLUKE 8050 digital multimeter, and an HP 6253 dual DC ...

EE 121: Digital Design Laboratory - web.stanford.edu
EECE 256 Digital Logic Design . Section 101/102 Term 1 - 2010/11. Final Exam in SRC A, 3:30-6:00, Tuesday Dec 7 th. Midterm Solution & old final questions posted. Exam covers Chap

UBC EECE 256 - Digital Logic Design
Midterm 1: after Boolean simplification Midterm 2: after RTL combinatorial components: Final Exam: Thursday, August 1, 1:00PM – 3:00PM in main lecture room: Primary Textbook: Frank Vahid, Digital Design with RTL Design, VHDL, and Verilog, SECOND EDITION, John Wiley, 2010. *First Edition also okay.

Digital Design 101 | DGLogic
Unit 9: Algorithmic State Machines, Introduction to Digital Logic Design. Lecture Notes: Unit 10: Basic Processor Architectures, Assembly Code. Lecture Notes: Homeworks, Quizzes, Exams. Homework 1: Solutions Homework 1: Quiz 1: Solutions Quiz 1: Homework 2: Solutions Homework 2: Quiz 2 (in-class students):

Fall 2013 - ECE238L: Computer Logic Design
Digital Design Laboratory Handout #18 Midterm Examination #1 Open book, open notes. Time limit: 75 minutes 1. (20 points) CMOS logic circuit. The CMOS circuit show in the flgure below computes a useful logic function. VDD Y X Z W F a. Fill in the function table for the above circuit. X Y Z F L L L L L H L H L L H H H L L H L H H H L H H H b.